RECONFIGURABLE NATO IV RF FRONT-END FOR SDR TERMINALS

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ABSTRACT

The paper describes the development process of a state of the art 2x2 MIMO NATO IV (4.4 GHz – 5 GHz) RF Front End.

First, requirements over the design are introduced, where it is important to emphasize that a low phase noise, fast synthesizer tuning time, high spurious rejection and fast AGC solution is pursued in the whole frequency band to allow the compatibility of the Front End with the most innovative wideband waveforms.

Second, the paper will present the architecture selected, that is based on COTS SISO WiMAX chipsets but synchronized among them to achieve a MIMO solution. The output frequency of these chipset will be moved into the desired NATO IV RF band by external RF circuitry. Digital control of the architecture is based on reprogrammable devices (FPGA) what allows complete flexibility and reduces the impact for its integration with any digital base band from hardware as well as from software standpoint.

Last but not least, an overview of implementation key challenges is provided: critical component selection based on validation by simulation and mock-ups implementation, key PCB implementation issues and the different microwave technologies utilized.

1. INTRODUCTION

The work described in this paper gathers and details all the development stages of a military NATO IV enabled RF Front-End, from technical specification to implementation, integration and trials.

The RF Front-End presented is intended to be integrated in a military vehicle for being used in tactical land deployments. To achieve this, considerations as easing the integration with different digital base band units and adaptability to support different waveforms have been taken into account. Software and hardware architectural details of the RF Front-End are provided in section 3 of this paper. First integration trials have been done considering a WiMAX (IEEE 802.16e compliant) digital base band unit.

Requirements coming from legacy and new state of the art waveforms (narrow and wide band) have been considered for the technical specification of the RF Front-End. The most challenging technical requirements and associated design decisions are outlined in section 2 of this paper.

Targeted frequency band is 4.4 GHz to 5.0 GHz, so the integrated equipment will be military NATO IV enabled. There is clear intention of migrating tactical radio systems to this frequency band in the near future. Emerging SDR platforms are expected to facilitate the introduction of cost-effective system in this band, allowing the support and provision of advanced services in LOS/NLOS Point-to-Point (PtP), Point-to-Multipoint (PtMP) and access deployments.

The RF Front-End has been designed to be integrated in a ruggedized enclosure adapted for vehicular usage and considering the fulfillment of EMI/EMC and environmental constraints (MIL STD 461 and MIL-STD-810). Both aspects have had impact in the implementation of the RF Front-End, such as layout (size, mechanical, gerbers..), components and PCB technology selection. All these mechanical and implementation considerations, whose most relevant aspects are introduced in section 0 of this paper, ensure the readiness of the implementation for field deployment.

The work presented in this paper has been performed in the scope the EUREKA project Broadpro [1] and has been co-funded by Spanish National Authority CDTI (*Centro para el Desarrollo Tecnológico e Industrial*) and Indra Sistemas S.A, with the Technological Centre GRADIANT acting as Indra's subcontractor.

2. REQUIREMENTS AND DESIGN DECISIONS

As introduced in section 1, main drivers of technical specification are to ease the integration of the RF Front-End with any SDR digital subsystem and to provide support to legacy and also to the newest and most advanced waveforms.

From a hardware standpoint these goals are translated into a very broad and stringent RF specification and an entirely flexible RF Front-End control approach. This flexibility is obtained through a FPGA-based proxy that implements the control and monitoring functions of the RF Front-End and an interface with the Digital Subsystem based on a high density connector with all the pins routed to the FPGA, providing full flexibility-

Software architecture of this FPGA component is based on a microblaze soft-core, embedded in the FPGA, integrated with specific verilog cores for time-constrained functionalities, such as AGC control or carrier frequency switching.

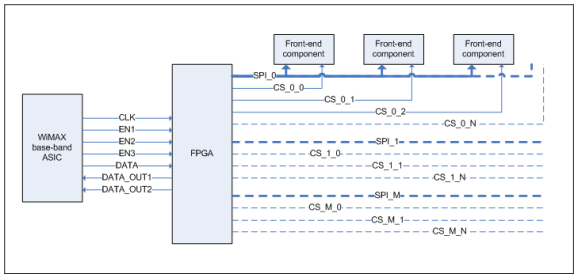

Figure 1. - RF-Front-End Control FPGA Proxy

More details of the hardware and software architecture of the RF Front-End are provided in section 3 of this paper.

As it has been **WiMAX** the first target waveform to be used and integrated with the RF Front-End, the proposed solution is based in the MAX2838 chipset [2]. This MAXIM transceiver is presenting a reconfigurable **RF channelization from 1.5 MHz to 28 MHz**, thus allowing the integration with other waveforms. The output frequency band of the MAXIM transceiver is from 3.3 GHz to 3.9 GHz so a hardware frequency converter module has been used to move the 600 MHz working bandwidth to **4.4 GHz to 5GHz frequency band.**

MIMO functionality is required. For this purpose, two transmission / reception branches, based on MAX2838 and working synchronously, are considered.

For testing the performances of the MAX2838, and confirm its selection, a specific MAX2838 mock-up has been implemented.

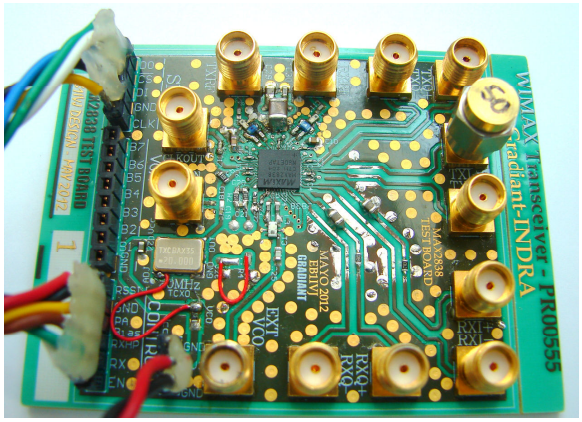

Figure 2. - MAX2838 mock-up

This MAX2838 test board has been used to analyze the compliancy with the requirements that rely on it, as frequency range, ripple, transmitted power, power control, harmonics and phase noise; and also for performing link tests, with modulated signals (DVB-T) , in transmission and reception.

A **transmission power from -20 dBm up to +24 dBm** is achievable in current design, with the possibility of **adjusting this power in 1 dB step**. This granularity, together with the RF control implementation based on FPGA, allows the integration of efficient waveform power control algorithms.

Transmitter output power is limited by the power consumption of the transmission power amplifier that is linked to the power provided to the RF Front-End (by the Digital Base Band). Current integration, with WiMAX baseband digital unit, limits the output power to +24 dBm but this figure could be incremented if more power is provided. Current integration with WiMAX standard is also considering a **back-off of 6dB** (suitable for multi-carrier modulations) that could be reduced in case of other kind of modulation is used, improving output power vs consumption performances. For testing the performances of the power amplifier selected (CREE CMPA2560025F, [3]), a specific mock-up (Figure 3) has been implemented.

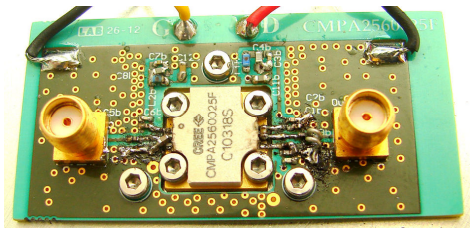

Figure 3. - Power Amplifier mock-up

Quite stringent linearity requirements, for transmission and reception, have been defined, specifying a **transmitter OIP3 of greater than + 35 dBm and a receiver IIP3 greater than + 25dBm**. Besides, high spectral purity is also required, with **spurious and harmonics rejection levels between 60 dB and 80 dB and a noise figure of less than 7 dB**. These requirements' fulfillment relies on the performance of the MAX2838 and the OL and mixer of the external hardware stage that makes the translation to NATO IV frequency band.

Down-conversion and Up-conversion mixers are based on Mini-Circuits Ultra Low Noise MMIC amplifier PMA-5453+ [4] and SIM-U712H mixers.

Specific mock-ups have been implemented for the up-conversion and down-conversion mixers (Figure 4), as well as for the local oscillator for assessing individually and in integration with the MAX2838 mock-up (Figure 2) the performances and confirming its selection.

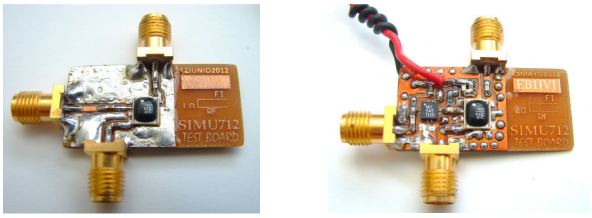

Figure 4. - Up-converter and down-converter mixers mock-ups

In order to support Fast Frequency Hopping waveforms, a carrier **frequency tuning time of less than 80 µs** is specified while keeping high performances in phase noise performance (-114 dBc @ 1 Mhz offset from carrier frequency), together with a **carrier stability equal or less than 1 ppm**. These requirements are affected by the MAX2838 and the external hardware to move to NATO IV frequency band.

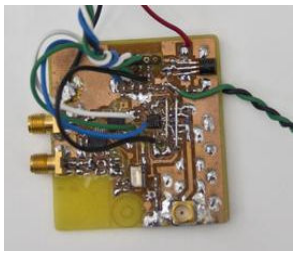

Figure 5. - Local Oscillator mock-up

The local oscillator is based on the Analog Device ADF4360 VCO [5] and a 20 MHz TCXO and a specific mock-up (Figure 5) has been implemented to assess its performances and confirm its selection. The TCXO selected ensures the fulfillment of the carrier stability requirement.

In order to allow the support to different waveforms (narrow and wide band waveform) a **broad reception dynamic range** has been specified (**94 dB**) that will be handled by a FPGA-based AGC.

The implementation of the AGC control unit in the FPGA embedded in the RF Front-End allows, on one hand, full reconfigurability of AGC dynamics for its adaptation to specific waveforms (amplitude modulation, phase modulations, multi-carrier schemes,...) and, on the other hand, the achievement of the **AGC attack time** specified (**< 36 µs**).

The stringent specification found for the AGC derives in a design decision of using logarithmic detectors that present, in front of RMS detectors, higher dynamic ranges and much better response time. Power detectors selected are Analog Device AD318. For AGC algorithm calculation, the MAX2838 RSSI detectors are also used.

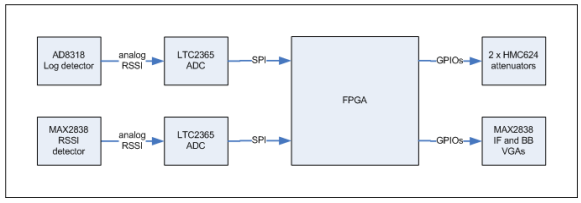

Figure 6. - AGC Components (for one branch)

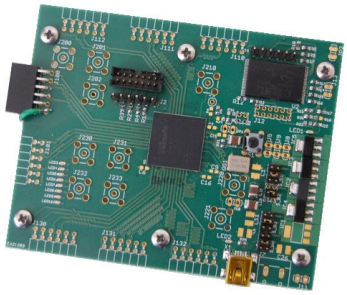

Figure 7. - FPGA mock-up

For initial validation of the firmware (microblaze and verliog cores components), a specific FPGA mock-up has been implemented that has been used in integration with the rest of the analog hardware mock-ups for architecture and design decision validation.

3. RF FRONT-END ARCHITECTURE

From previous section in which HW and SW requirements, and derived design decision, for the MIMO NATO Band IV RF Front End are detailed, present section is focused on the RF Front-End Architecture description.

Present section is structured in two main sub-sections: HW architecture of the RF Front-End and SW/FW Architecture as an enabler of the RF Front-End full reconfigurability.

A. HARDWARE ARCHITECTURE

In Figure 8 it is presented a high level diagram of the RF Architecture defined for the MIMO NATO Band IV RF Front-End.

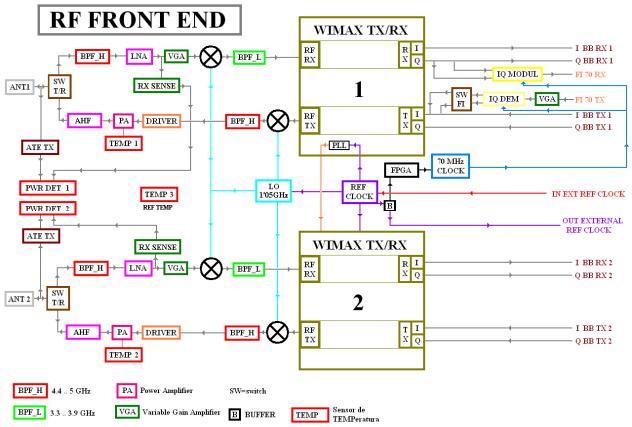

Figure 8. - HW Architecture

RF Architecture design is based on the usage of commercial WiMAX direct conversion transceivers typically used in WiMAX certified equipments. Specifically, RF architecture selected considers the usage of two MAX2838 transceiver chipsets working synchronously, due to the MIMO requested architecture, which work in the 3.3 to 3.9 GHz commercial band for WiMAX communications.

Frequency band requirement for the MIMO RF Front End is to operate in NATO Band IV (from 4.4. to 5 GHz), therefore is requested to add a frequency conversion stage to move the original 600 MHz chipsets bandwidth to the desired frequency band.

MIMO architecture requirement implies the necessity to duplicate TX and RX chains, besides a critical time control of both branches.

First, HW modules making up the two down-conversion branches of the RF Front End are described. RF Front End operating in RX performs a down-conversion from NATO IV band to 3.3 – 3.9 GHz frequency band to subsequently feed MAX2838 chipset. Hereinafter. HW modules that go though the received signal path are briefly described
:

- **Unidirectional High Band Pass Filter** for global selectivity of 600 MHz in NATO IV band (from 4.4 to 5.0 GHz). Due to the reduced space available for filters, the need to provide MIMO support, the conversion architecture selected and stringent RF performance, an ad-hoc manufacture of the filters of this RF Front End has been needed.
- **RF Switch** for selecting the correct branch (TX or RX).
- **Low Noise Amplifier** to obtain a relevant gain factor and keep controlled noise factor parameter.
- **Power Detector module**, which is in charge to detect the in band power signal. These estimations are used as inputs for correct operation of the Automatic Gain Control (AGC).
- **Variable Gain Amplifiers,** which are in charge of selecting the appropriate gain or attenuation in order to feed mixer with the proper signal level (important to achieve optimum inter-modulation figures and fulfill requirements). These amplifiers are controlled by the FW architecture.
- **Mixer**, which is in charge of the down-conversion process. 1050 MHz reference local oscillator, properly synchronized in both MIMO branches, is used for the mixing process.
- **Unidirectional Low Band Pass Filter**, which is in charge of selecting the 3.3 to 3.9 GHz native frequency band for the WiMAX transceiver chipset.

Regarding TX operation, TX branch is responsible for moving native frequency band of WiMAX Transceiver (from 3.3 GHz to 3.9 GHz) to NATO IV frequency band. Both up-conversion branches are made up of the following RF modules:

- **Mixer**, which is in charge to mix RF signal from WIMAX transceiver and 1050 MHz local oscillator to move operative frequency band to Nato Band IV. There is a mixer module in each TX branch.
- **Unidirectional High Band Pass Filter** applied to the mixer output previously to any amplification stage.
- **Pre-Amplification stage (driver amplification)**, which is in charge to apply the required gain factor to drive correctly the power amplifier.

- **Power Amplifier,** providing the amplification stage in charge of obtaining the maximum output level according requirements.
- **RF Switch** for selecting the TX or the RX branch.
- **Unidirectional Anti-harmonic Filter,** with low insertion losses
- **Power Detector module** feed by the transmission signal after the fixed required attenuation to not affect power detector and avoiding any kind of reflection problem.

Apart from TX and RX branches, RF architecture also contains the following modules:

- **Reference Clock circuit** which is in charge to manage the reference clock. This reference clock can be provided form an external source and it is distributed to all RF components using it (WiMAX transceiver chipsets, local oscillator and FPGA). In case no external reference is present at input, TXCO provides its internal reference clock, fulfilling stability requirements. External reference has always priority against internal reference.
- **Local Oscillator**, which is in charge to generate the 1.1. GHz tone input for the up-mixers and down-mixers. Therefore, output tone needs to be amplified and split for the 4 mixers.
- **Temperature sensors** included in the RF architecture to control operation temperature of the two power amplifiers and in specific and critical.

B. FIRWARE/SOFTWARE ARCHITECTURE

Apart from the Hardware Architecture, FW/SW architecture allows fully reconfigurability of the RF Front End, easing RF Front End integration with different SDR Platforms.

Firmware/Software architecture is based on the usage of a FPGA device providing a registers map accessible, using a standard SPI bus, by the SDR platform to configure, control and monitor all RF Front End parameters.

Figure 1 depicts a high level diagram of the HW/SW Architecture designed for the MIMO NATO IV RF Front-End.

Selected FPGA FW/SW architecture is based on a MicloBlaze soft-core CPU processor which is in charge to manage a SPI bus for communication between external SDR platform and MicroBlaze CPU.

Additionally, as can be seen in Figure 1, other SPI buses are managed by the MicroBlaze processor to support configuration and control of the RF Front-End:

- **RF Subsystem General Control** (with the digital base band): activation of the RF Front End, deactivation of specific branch (for MIMO or SISO operation mode), etc.
- **Local Oscillators** control.
- **Transmission power control.**
- **VGAs** control and monitoring supporting AGC capability.
- **ADCs** for power detection and analog signal provision to SDR platform.
- **AGC parameterization.**
- **Temperature sensors** control.
- **Clock Reference** Control.

SW/FW architecture is implemented on FPGA device XA Spartan-6 Family, which support and extended temperature range compared with typical FPGA from Spartan-6 family. This extended range feature has been needed to allow the system to fulfill MIL-STD standards.

4. IMPLEMENTATION DETAILS

RF Front-End has been designed for its integration on a ruggedized enclosure, together with the digital base band hardware, ready to be installed in a military vehicle

Figure 9 shows the mechanical design of this ruggedized enclosure and the space reserved for the RF Board and the Digital Baseband Board. .

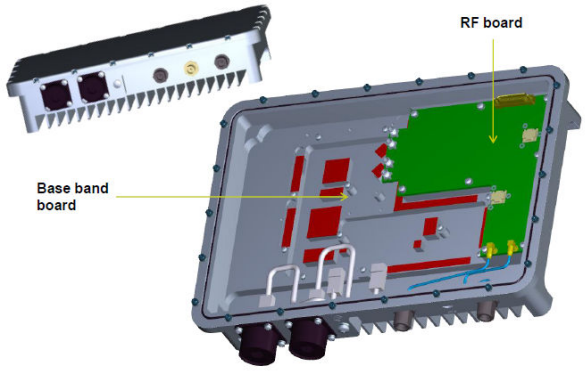

Figure 9. - Ruggedized Enclosure

The space limitations have impacted in components selection that has derived in the need of custom implementation of the high-band filters (4.4 GHz – 5 GHz) and in the decision of reusing components for transmission

and reception branches, feasible thanks to the half-duplex characteristics of the transceiver.

The system, integrated in the enclosure, must fulfill MIL-STD environmental and EMI/EMC requirements, presenting an operational temperature range from -40ºC to +65 ºC.

Specific power dissipation, vibration, shock and stress analysis have been performed over the system.

Figure 10 shows some details of the outcomes obtained in the thermal analysis performed.

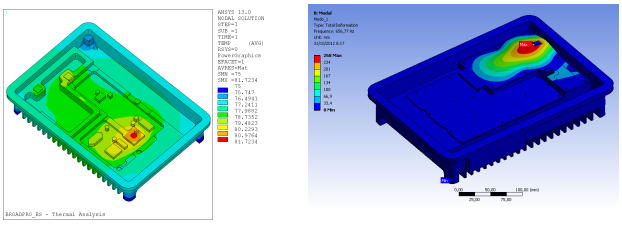

Figure 10. - Thermal and structural analysis (some results)

Compliancy with MIL-STD standards has been obtained constraining the placing of most critical components as, for example, FPGA and Power Amplifiers and implementing in the enclosure mechanics specific heat dissipation towers for the critical components.

RF Front-End FPGA has been selected with extended temperature range and in contact with a specific dissipation tower. This ensures the compliancy with MIL-STD standards, even in the case of control FW evolution for its adaptation to other waveforms.

Due to the hard restrictions in this project, a special 6-layer PCB was designed. It uses a symmetrical stack-up, using microwave low loss RO4350 cores at the top and bottom sides, and a standard central FR4 core, being this glued by intermediate prepegs to the RF cores. Only one core is used for RF devices, but symmetrical stack-up avoid PCB bending due to differential physical properties against temperature, as in a bimetallic thermostat.

Double side components placement is needed, being impossible the design if only one side is used.Via hole managed levels are 3:

- A full through via hole level, connecting the 6 layers, used to interconnect digital and analog parts and for general grounding and shielding.
- A 1-2 level, reserved for RF devices on the top layer
- A 3-6 level, used mainly for bottom layer digital devices, but too in striplines.

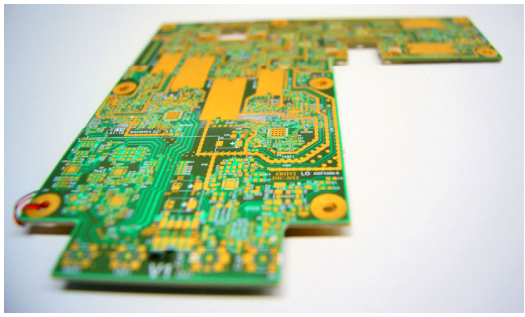

Figure 11. - NATO IV RF Front-End PCB

All digital noisy devices, as FPGA, charge pump, ADCs, high voltage switched power supply for the power amplifier, etc., are in the bottom side, while analog RF signals are mainly in the top side, with ground plane keeping away the noisy part from the analog parts.

Special care is needed when defining via holes levels, because each of this level requires a manufacturer re-metallization in the copper layer, for metallic deposition in the via-hole inner cylinder. Each of this re-metallization adds some tens of um in the copper thickness, and we need to take in account this when we are using 10 mils RF substrate cores. Copper is thicker now, and this modifies RF tracks impedance.

150um tracks are used to manage high density routing for FPGA pin-out. Via-hole re-metallization process limits available resolution, making a little difficult the routing near FPGA. Differential lines were used in the base band signal to avoid noise. Microstrip lines in the external cores are used as transmission lines, using stripline in the internal layers to provide RF crossings and in order to keep highly shielded some critical signals as the 4/3 RF carrier used for MAX2838 synchronization in MIMO operation. This signal is not a big problem in the MAX2838 native frequency band (3300-3900MHz) but go across all the target NATO IV frequency band (4400-5000MHz), so it can be a excellent auto-jammer if care is not taken. StripLine provides a big shielding, 90 dB or more, while microstrip at 5GHz microwave in our design can only warrants values around 60 to 65 dB for shielding between lines. Stripline higher performance is coming from the 2 ground plane around the active line, quite similar to a coaxial structure.

It can be summarized this design as a hybrid digital-analog prototype, 6 level multilayer PCB and with both sides components, being really a not trivial task requiring enough engineering skills, managing old and classic concepts and others quite new, mixing RF and FPGA world in a real prototype

Figure 12 shows final implantation of the NATO IV RF Front-End.

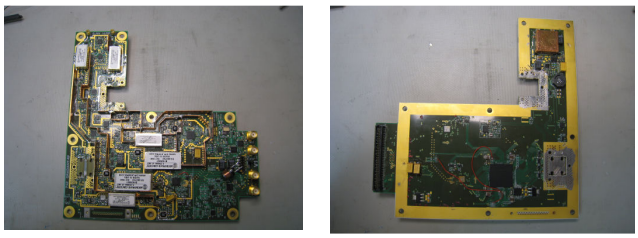

Figure 12. - NATO IV RF Front End (final implementation)

5. CONCLUSIONS

In this paper, the challenges found when developing a fully reconfigurable, multi-mode, SDR-ready and NATO IV capable RF Front End has been detailed.

Architectural design decisions, component selection process and implementation constraints has been described in front of the stringent set of requirements that have to be fulfilled. The presented RF Front-End is intended to be integrated with the most innovative state-of-the-art waveforms.

Feasibility has been demonstrated through its implementation and validation in a vehicular oriented form factor, integrated with a WiMAX standard based digital Base Band unit.

6. REFERENCES

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[3] CMPA2560025F, 25W 2500 – 6000 MHz, GaN MMIC Power Amplifier (http://www.cree.com/~/media/Files/Cree/RF/Data%20Sheets/CMPA2560025F.pdf)

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